IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Conf. No.: 9391
Kazunari KURITA et al.	Art Unit: 1792
Application No.: 10/576,321	Examiner: Kunemund, Robert M.
Filed: 04/19/2006	Attorney Dkt. No.: 12054-0059

For: PROCESS FOR PRODUCING HIGH-RESISTANCE SILICON WAFERS AND PROCESS FOR PRODUCING EPITAXIAL WAFERS AND SOI WAFERS

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request reconsideration of the rejections made in the Office Action dated July 23, 2009.

In review, the Examiner has made a new rejection citing EP 1087471 to Abe, JP 2000-344598 to Ikari, and United States Published Patent Application No. 2004/0102056 to Tobe et al. (Tobe) to allege that the claims are obvious under 35 U.S.C. § 103(a) . In the rejection, the Examiner alleges that Abe teaches the claimed method except for the carbon limitation and the third annealing step. Ikari is cited to allege that the claimed carbon concentration is known and Tobe is cited to allege that a third annealing step is disclosed after a high temperature annealing. The Examiner indicates that the desire to create final properties is sufficient reasoning to modify Abe to employ the carbon concentration of Ikari and the third heating step of Tobe.

Applicants submit that the Examiner has not established a *prima facie* case of

obviousness and the rejection as applied to the claims must be withdrawn. The traverse of the rejection is set out below under the headings of the Invention and the cited prior art.

INVENTION

In review, claim 1 describes a process as follows:

> A process for producing high-resistance silicon wafers wherein it comprises
>
> subjecting silicon wafers obtained by the Czochralski method and having a resistivity of 100 Ωcm or above, an initial interstitial oxygen concentration of 8×10^{17} atoms/cm^3 or above (ASTM F 121-1979) and, further, a carbon concentration of 5×10^{15} to 5×10^{17} atoms/cm^3 (ASTM F 123-1981)
>
> to first heat treatment consisting in 0.5 to 5 hours of heat treatment at 850 - 1000°C employing a rate of heat-up of 0.5 to 10°C/minute at least in the temperature range of 700 - 850°C and, further,
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> to second heat treatment consisting in 1 to 2 hours of heat treatment at 1150°C or above followed by
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> subsequent lowering of the temperature and heat treating at 1000 - 1150°C for 2 to 10 hours.

As can be seen from claim 1, the inventive method involves the treatment of a particular wafer grown by the CZ method. The treatment entails a first heat treatment at a first temperature and a second heat treatment. The second heat treatment entails heating at a second temperature greater than the first temperature and then a temperature reduction to a temperature lower than that used initially in the second heat treatment.

The resistivity of high-resistance silicon wafers is greatly influenced by the amount of oxygen donors generated. In the case of p-type wafers, in particular, the increase in the amount of oxygen donors formed may result in the inversion to n-type

semiconductors and/or great changes in resistivity. When the resistivity of the wafer inside becomes too low due to a decrease in resistivity, the amount of current passing through a place deeper than the region for device manufacture increases and causes energy losses and/or produces current noises, thus markedly deteriorating the device characteristics. The oxygen donors formed include thermal donors (old donors) estimated to be oxygen clusters, and new donors considered to be minute precipitates in initial form. Presumably, these oxygen donors are dissolved or undergo a modification in the manner of bonding and electrically neutralized during the heat inventive treatments and, accordingly, their formation is suppressed. See paragraphs [0027-0028] of Applicants' published application.

As a result of various investigations concerning oxygen donors, the present inventors, premised on the heat treatment employed in device manufacture, could reveal the permissible limit level of oxygen donors formed in the wafer inside after such heat treatment. Thus, in the case of high-resistance wafers with an initial resistance of 100 Ωcm or above, when the amount of oxygen donors formed as found after heat treatment in the device manufacture is 1×10^{13} atoms/cm^3 or below, the wafer resistivity can be maintained thereafter at a high level, the resistance values can be prevented from changing greatly, and the inversion to n-type, energy losses and/or current noises can be prevented from occurring.

Referring again to claim 1, the first heat treatment is required to be carried out at 850-1000 °C for 0.5 to 5 hours while adjusting the heat-up rate to 0.5 to 10 °C/minute at least within the temperature range of 700-850 °C. In this first heat treatment, the formation of minute precipitation nuclei and the growth thereof are

promoted by the controlled heat-up procedure or ramping from a low temperature, see paragraph [0055] of Applicants' published application.

In the second heat treatment, it is essential that 1 to 2 hours of heat treatment at 1150 °C or above be followed by temperature lowering to 1000 to 1150 °C and further followed by 2 to 10 hours of heat treatment in the lowered temperature range. The second heat treatment is carried out for the purpose of outward diffusion heat treatment and for promoting the growth of precipitates, see paragraph [0056] of Applicants' published patent application.

Tobe

In the rejection, the Examiner contends that Tobe teaches the third heat treating step, i.e., the lowering of the temperature from the claimed 1 to 2 hours at 1150 °C or above to 1000-1150 °C for 2 to 10 hours.

Tobe relates to control of the amount of oxide precipitation in a silicon wafer. Tobe teaches performing rapid heat treatment (RTA treatment) to a silicon wafer with a rapid heating-rapid cooling apparatus. As a result of this treatment, atomic vacancies are injected from a surface of the wafer to form a maximum position of an atomic vacancy concentration in a depth direction in the vicinity of the surface of the wafer. Then, a heat treatment (post annealing) is performed to move the maximum position of the atomic vacancy concentration in the vicinity of the surface of the wafer into the inside of the wafer, see claim 1 thereof. Presumably, the Examiner is considering the post anneal treatment to be one that uses a lower temperature than the RTA treatment and concludes that one of skill in the art would

use the post annealing treatment of Tobe in the method of Abe.

Tobe's two step heat treatment is performed in a temperature range of 1100-1350 °C, followed by post annealing in a temperature range of 700-1050 °C.

From the above, it is plain to see that the two step heat treatment, i.e., RTA treatment followed by a post anneal is not in the least similar to the two step treatment of claim 1. In Tobe, oxygen precipitation is performed after the RTA treatment. This, in effect, is a first high temperature heating followed by a lower temperature heating, which corresponds to the post anneal heating.

In contrast, the process of claim 1 has a first heat treating step which is a low temperature heating followed by a second heat treating step that uses a higher temperature. While it is true that the second heat treating step also employs a temperature lowering, this does not change the fact that the claimed process starts with a low temperature heat treatment followed by a high temperature heat treatment. This is the exact opposite of Tobe.

In the rejection, the Examiner assumes that Abe teaches the claimed low temperature heat treatment followed by a high temperature heat treatment. If this is the case, why would one of skill in the art look to Tobe, which starts out with a high temperature heat treatment and use just the second step of Tobe in Abe's method. This reasoning has no legitimate factual basis and cannot support the conclusion of obvious by modifying Abe according to Tobe.

Further, the first heat treatment step of claim 1 involves an adjustment of the heat-up rate in the temperature range of 700-850 °C. This adjustment results in the formation of oxygen precipitation nuclei within the wafers and improvement

of the density of oxygen precipitation nuclei, see paragraph [0058] of Applicants' published patent application. This heating up is not in the least taught or suggested in Tobe.

To recap, the present invention is characterized by the combination of first and second heat treatments. The first heat treatment is includes a heat up or ramping that is carried out in a controlled manner. The second heat treatment involves a first higher temperature treatment and then a second lower temperature treatment. Tobe is completely unrelated to this sequence of steps.

Again, the Examiner is merely taking the post anneal step of Tobe and saying that it would be obvious to employ this step in the process of Abe. This allegation is without the articulated reasoning required to support a rejection based on 35 U.S.C. § 103(a).

In the rejection, the Examiner cites the desire to obtain desired properties. However, no mention is made of what properties are desired or why one would employ just one of the two heat treating steps of Tobe in the different processing of Abe, as is explained in more detail below. This is another error in the rejection in that the Examiner has not provided the proper reasoning for the modification of Abe. Thus, a *prima facie* case of obviousness is not established using Tobe and the rejection as applied to claim 1 must be withdrawn.

Abe

Abe relates to a silicon wafer having a resistivity of 100 Ωcm or more. Abe teaches a device production heat treatment at 350-500 °C, which is then followed

by an oxygen precipitation heat treatment. Following this procedure means that the resistivity of 100 Ωcm or more can be maintained.

In Abe's oxygen precipitation heat treatment, a high temperature heat treatment at 1100 °C or higher is performed in its first step so as to diffuse outward the interstitial oxygen in the surface of the wafer, see paragraph [0052] of Abe. This is different from the condition of the claimed two step heat treatment.

In fact, the Examiner has made an error in interpreting Abe. In the rejection the Examiner states:

> The Abe references teaches a method of producing a high-resistance silicon wafer having a resistivity of 100 Ωcm or more, oxygen concentration of $14x10^{17}$ atoms/cm^3 or more, remaining oxygen concentration of $12x10^{17}$ atoms/cm^3 or less by performing heat treatment performed at 700-900 °C for 4 for 5 hours or more, a heat treatment performed at 950-1050 °C for 10 hours or more, a heart (sic) treatment performed at 1100-1250 °C for 1-5 hours, and a density of a grown-in defect of $1x10^3$/cm^3.

The rejection is in error for the simple reason that the processing alleged to be that of Abe's is, in fact, not the disclosure of Abe. This along means that the entire basis of the rejection is flawed and a *prima facie* case of obviousness cannot exist. It appears that the Examiner has inadvertently referred to application no. 10/512,405 (PCT/JP03/004866), which was cited in one of the previous double patenting rejections. The quotation above can be found on page 3 of the Office Action dated December 18, 2007.

Still referring to Abe, the actual processing of Abe can be gleaned from Figure 3, thereof. In this processing, the high temperature heat treatment is performed in a first step. In contrast, claim 1 calls for a low temperature heat

treatment in combination with a second high temperature heat treatment. More particularly, the first heat treatment of claim 1 is carried out in a controlled manner (ramping), and is combined with the second high temperature heat treatment, which involves two temperatures, the initial one higher than the later one. In addition, the heating conditions, including the temperatures are different between Abe and claim 1.

What this means is that Abe does not teach the process of claim 1 but for a "third heat treatment" and "carbon concentration" as alleged in the Office Action and a *prima facie* case of obviousness cannot be said to exist, regardless of the teachings of the secondary references. Put another way, since Abe does not teach the claimed process but for the third heat treatment step, even if Tobe were combined with Abe, the processing of claim 1 would still not exist and obviousness would not be established. The same reasoning applies for the reliance on Ikari.

Ikari

While Ikari is cited to allege that the claimed carbon concentration is obvious, this reference still does not make up for the failings in Abe and Tobe. That is, Ikari relates to the production of wafers for MOS devices having precipitation defects in high density at the center of the thickness direction so as to exert an excellent gettering capability. To achieve this, Ikari subjects the obtained silicon semiconductor substrate to heat treatment in a non-oxygenated atmosphere in a temperature range of 1000-1300 °C for an hour or more, see claim 2 thereof. This means that Ikari's heat treatment is not the same as that found in claim 1 and that one of skill in the art cannot arrive at the claimed two step heat

treatment based on the teachings of Ikari.

Summary

To recap, the Examiner has not established a *prima facie* case of obviousness since the primary reference to Abe does not teach the processing alleged to be present in the rejection. Since Abe was used as a principal basis of the rejection and the Examiner has misinterpreted Abe's teachings, the rejection fails. The rejection is also flawed since the heat treatment of Tobe is not similar to that of the invention and no articulated reasoning was given to support the conclusion that it would be obvious to use one of the heat treating steps of Tobe in the process of Abe. Finally, since Abe does not teach the fundamental aspects of claim 1, even if Tobe were combined with Abe, the limitations of claim 1 would still not exist. Ikari does not make up for the failings in Abe and Tobe and even if this reference were combined with Abe, a *prima facie* case of obviousness would not exist. Since claim 1 is patentable over the applied prior art, its dependent claims are also in condition for allowance.

Accordingly, the Examiner is requested to examine this application and pass all pending claims onto issuance.

Title of the Invention

Lastly, Applicants filed a Preliminary Amendment on April 19, 2006 with the initial application. In said Amendment, Applicants edited the Title of the Invention. Upon review of the PTO website (PAIR), Applicants noted under the Bibliographic Data that the Title had been changed, however, the term "(as amended)" was included. Please see the

attached PAIR printout. As this was not a clerical error made by the Applicant, it is respectfully requested that the Title be corrected by the U.S. Patent & Trademark Office.

Conclusion

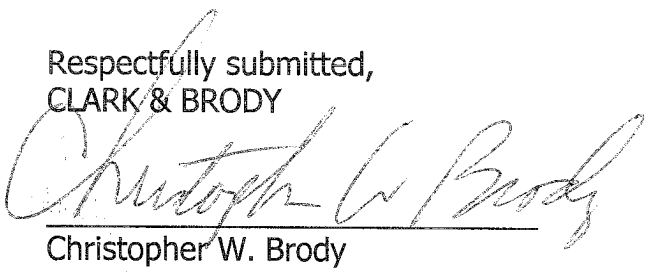
If the Examiner believes that an interview would be helpful in expediting the allowance of this application, the Examiner is requested to telephone the undersigned at 202-835-1753.

Again, reconsideration and allowance of this application is respectfully requested.

The above constitutes a complete response to all issues raised in the Office Action dated July 23, 2009.

No fees are believed to be due in connection with this filing. However, please charge any fee deficiencies to Deposit Account No. 50-1088.

Respectfully submitted,
CLARK & BRODY



Christopher W. Brody
Registration No. 33,613

Customer No. 22902
1090 Vermont Avenue, N.W., Suite 250
Washington DC 20005
Telephone: 202-835-1111
Facsimile: 202-835-1755

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10/576,321	Process for producing high-resistance silicon wafers and process for producing epitaxial wafers and soi wafers (as amended)	10-21-2009::11:34:38

Bibliographic Data

Application Number:	10/576,321	Customer Number:	22902
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Title of Invention:	Process for producing high-resistance silicon wafers and process for producing epitaxial wafers and soi wafers (as amended)

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